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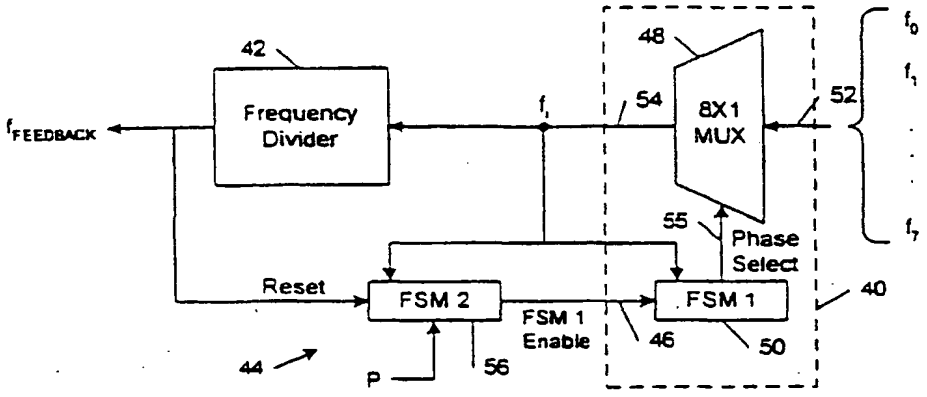
(54) Title: HIGH RESOLUTION, LOW JITTER FREQUENCY SYNTHESIZER



(57) Abstract: Improved systems and methods for synthesizing frequencies with high resolution and low jitter are described. In one aspect, a frequency synthesizer for producing a series of output signal pulses spaced-apart by a characteristic period is described. The frequency synthesizer includes a phase-locked loop having a multiphase counter configured to produce a feedback signal pulse shifted in time by a programmable fraction of the output signal period relative to a period corresponding to a programmable number of output signal pulses. In another aspect, a phase shifter is configured to provide an over sampling clock signal with a frequency greater than the frequency of the output signal. In another aspect, the frequency synthesizer includes a phase-locked loop with a charge pump having a pull up current source, a pull down current source, and an equalization circuit programmable to substantially offset mismatch between the pull up current source and the pull down current source.

WO 02/27938 A2

HIGH RESOLUTION, LOW JITTER FREQUENCY SYNTHESIZER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. Application Serial No. 09/675,998, filed on even date herewith, by Sasan Cyrusian, and entitled "Phase Detecting," which is incorporated herein by reference.

TECHNICAL FIELD

This invention relates to systems and methods for synthesizing frequencies with high frequency resolution and low jitter.

BACKGROUND

Frequency synthesizers are used in a wide variety of applications, including wireless communications (e.g., digital cellular communications) and magnetic read/write channels for disk drive applications. Frequency synthesis typically involves generating from a fixed-frequency reference signal a plurality of output signals over a wide range of frequencies. There are two main approaches to frequency synthesis, direct and indirect. In direct frequency synthesis, the fixed-frequency reference signal is processed (e.g., by a frequency divider or a frequency multiplier) to generate an output signal of a desired frequency. In indirect frequency synthesis, a tunable frequency source (e.g., a voltage controlled oscillator (VCO)), which is locked to the fixed-frequency reference signal, generates an output signal of a desired frequency. In a common indirect frequency synthesis approach, a phase-locked loop with a frequency divider in the feedback path tunes the VCO frequency (f_{VCO}) to a multiple of the reference frequency (f_{REF}). For example, in one system, divide-by-N logic divides the VCO output signal frequency (f_{VCO}) by N to produce a feedback signal with a frequency f_{VCO}/N. A phase detector tunes the VCO until the phase of the feedback signal matches the phase of the reference signal. By changing the value of N, the output signal produced by the VCO may be changed in frequency steps equal to the reference frequency (i.e., $f_{VCO} = N \cdot f_{REF}$). Thus, in this approach, in order to increase the frequency resolution of the synthesizer, the frequency of the reference signal must be decreased. However, the bandwidth of the phase-locked loop must decrease to accommodate a lower reference frequency, increasing the time needed to lock to a particular frequency and increasing the noise level (jitter) in the output signal.

SUMMARY

The invention features improved systems and methods for synthesizing frequencies with high frequency resolution and low jitter.

In one aspect, the invention features a frequency synthesizer for producing a series of output signal pulses spaced-apart by a characteristic period. The inventive frequency synthesizer comprises a phase-locked loop having a multiphase counter configured to produce a feedback signal pulse shifted in time by a programmable fraction of the output signal period relative to a period corresponding to a programmable number of output signal pulses.

Embodiments may include one or more of the following features.

The phase-locked loop preferably comprises an output signal generator (e.g., a ring oscillator) configured to produce multiple phases of the output signal. The multiphase counter preferably comprises a phase selector coupled to the output signal generator and configured to output a selected phase of the output signal based upon a programmable input value. The phase selector may include a multiplexer coupled to receive the multiple phases produced by the output signal generator. The phase selector also may include a finite state machine coupled to the phase selector and having one state for each of the multiple phases of the output signal. The finite state machine preferably is configured to switch states in response to a pulse of the selected phase of the output signal received from the multiplexer.

The multiphase counter may further include a delay module (e.g., a frequency divider) coupled to the phase selector and configured to produce a feedback signal pulse after a programmable number of output signal pulses have been received from the phase selector. The multiphase counter also may include a controller coupled to the phase selector and configured to selectively enable and disable the phase selector. The controller preferably is configured to enable the phase selector upon receipt of a feedback signal pulse from the delay module, and to disable the phase selector after a programmable number of output signal pulses have been received from the phase selector.

In another aspect of the invention, a phase shifter is coupled to the output signal generator and is configured to provide an over sampling clock signal with a frequency greater than the frequency of the output signal.

In another aspect, the invention features a frequency synthesizer that includes a phase-locked loop with a charge pump having a pull up current source, a pull down current source, and an equalization circuit programmable to substantially offset mismatch between the pull up current source and the pull down current source.

The equalization circuit preferably comprises a pull up offset cancellation current source and a pull down offset cancellation current source respectively coupled in parallel with the pull up current source and the pull down current source.

Among the advantages of the invention are the following.

The invention provides a power efficient low jitter frequency synthesizer with a high frequency resolution. The invention allows a higher reference frequency to be used for controlling the output frequency. This feature allows the size of the loop filter in the phase locked loop to be reduced and, consequently, reduces the time needed for the frequency synthesizer to lock to a particular output frequency. The invention also reduces jitter in the charge pump by substantially canceling mismatches between the pull up current source and the pull down current source.

Other features and advantages of the invention will become apparent from the following description, including the drawings and the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a frequency synthesizer, including a multiphase VCO, a multiphase counter and a charge pump.

FIG. 2 is a block diagram of the multiphase VCO of FIG. 1.

FIG. 3 is a block diagram of the multiphase counter of FIG. 1.

FIG. 4A is a detailed block diagram of the multiphase counter of FIG. 3.

FIGS. 4B and 4C are state diagrams of two state machines operable in the multiphase counter of FIG. 4A.

FIG. 5 is a block diagram of the charge pump of FIG. 1.

FIG. 6 is a block diagram of the frequency synthesizer of FIG. 1 configured to supply a read clock and a write clock for a magnetic read/write channel.

DETAILED DESCRIPTION

Referring to FIG. 1, in one embodiment, a frequency synthesizer 10 includes a phase-locked loop 11 with a phase detector 12, a charge pump 14, a loop filter 16, a multiphase voltage-controlled oscillator (VCO) 18, and a multiphase counter 20. In operation, phase detector 12 generates frequency adjustment signals V_{UP} and V_{DOWN} in response to a detected phase difference between a fixed-frequency reference signal (having a frequency f_{REF}) and a feedback signal (having a frequency $f_{FEEDBACK}$), which is produced at the output of multiphase counter 20. The reference signal may be generated by any stable frequency

source (e.g., a crystal oscillator). In response to frequency adjustment signal V_{UP}, charge pump 14 charges a capacitor in loop filter 16 with a current $I_{PULL\ UP}$. In response to frequency adjustment signal V_{DOWN}, charge pump 14 discharges the loop filter capacitor with a current $I_{PULL\ DOWN}$.

As explained in detail below, the resulting voltage (V_{CTL}) at the output of loop filter 16 controls the frequency (f_{OUT}) of the output signal generated by multiphase VCO 18. Multiphase counter 20 feeds a down-converted version of the output signal back to the input of phase detector 12. In particular, based on the programmable integer parameters N and P, multiphase counter generates from the output signal a down-converted feedback signal with a frequency ($f_{FEEDBACK}$) given by the following equation:

$$f_{FEEDBACK} = f_{OUT} / (N - P/x) \quad (1)$$

where x is the number of phases of the output signal generated by multiphase VCO 18. By substituting f_{REF} for $f_{FEEDBACK}$ and solving for f_{OUT}, the output signal frequency (f_{OUT}) may be expressed in terms of the reference frequency (f_{REF}) as follows:

$$f_{OUT} = f_{REF} \cdot (N - P/x) \quad (2)$$

Thus, by proper selection of parameters N and P, a wide variety of output signal frequencies may be generated with a resolution of f_{REF}/x, a resolution that is x times greater than a conventional divide-by-N phase-locked loop frequency synthesizer.

Referring to FIG. 2, in one embodiment, multiphase VCO 18 includes a ring oscillator 30 formed from a plurality of voltage-controlled differential delay cells 32, 34, 36, 38. Each delay cell 32-38 includes a differential input and two outputs (inverting and non-inverting). The delay through each cell 32-38 is substantially the same and is controlled by the control voltage (V_{CTL}) produced at loop filter 16. Since the overall delay through all of the cells 32-38 determines the oscillation period of ring oscillator 30, control voltage V_{CTL} controls the frequency of the signal produced by multiphase VCO 18. By tapping the outputs of each of delay cells 32-38, multiple, equally spaced phases ($f_0, f_1, \ldots, f_7$) of the output signal may be obtained. One of these phases is selected as the output signal of frequency synthesizer 10.

In other embodiments, multiphase VCO 18 may include any suitable oscillator or delay line that produces multiple phases of the output signal. For example, in one embodiment, multiphase VCO 18 may include a delay-locked loop. Furthermore, a different

number of delay cells may be incorporated into ring oscillator 30 to increase or decrease the number of output signal phases generated by multiphase VCO 18.

Referring to FIG. 3, multiphase counter 20 includes a phase selector 40, a frequency divider 42, and a controller 44. Phase selector 40 is coupled to multiphase VCO 18 and is configured to output a selected phase of the output signal based upon a programmable value (P) that is applied to the input of controller 44, which applies a phase selection signal 46 to an input of phase selector 40. Frequency divider 42 divides the frequency of the selected phase by N to produce a feedback signal with a frequency ($f_{FEEDBACK}$), which is expressed in terms of the output signal frequency (f_{OUT}) in equation (1) above. Frequency divider 42 may be any type of counter or divider, such as a shift register, a binary counter, or another conventional counter.

Referring to FIGS. 4A, 4B and 4C, in one embodiment, phase selector 40 is implemented by a multiplexer 48 and a finite state machine 50 (FSM1). Multiplexer 48 has an input 52 for receiving each of the phases (f_0, f_1, . . . , f_7) of the output signal and a single output 54 for outputting a selected one of the output signal phases (f_i); the selected phase is determined by a phase select signal 55 generated by finite state machine 50. Finite state machine 50 has a state for each of output signal phases (FIG. 5B), with each state producing a respective phase select signal 55. In this embodiment, controller 44 is implemented as a finite state machine 56 (FSM 2) that has two states: an enable FSM 1 state that enables finite state machine 50 to switch states; and a disable FSM 1 state that disables the state switching of finite state machine 50 (FIG. 4C). Finite state machines 50, 56 and frequency divider 42 are clocked by the rising pulse edges of the selected phase produced at output 54 of multiplexer 48. In operation, frequency divider 42 outputs a feedback signal pulse after every N clock pulses of the multiplexer clocking signal. The feedback signal pulse is applied to a reset input of finite state machine 56. Upon receipt of the reset signal, finite state machine 56 switches from the disable FSM 1 state to the enable FSM 1 state. When enabled, finite state machine 50 switches from state-to-state on the rising edge of each multiplexer clock pulse, as shown in FIG. 5B. After P clock pulses have been received from the output of multiplexer 48, finite state machine 56 discontinues the FSM 1 enable control signal 46, fixing the phase produced at output 54 of multiplexer 48. The resulting period ($T_{FEEDBACK}$) between frequency divider pulses is given by:

$$T_{FEEDBACK} = N \cdot T_{OUTPUT} - (P/x) \cdot T_{OUTPUT} = T_{OUTPUT} \cdot (N - P/x) \qquad (3)$$

where T_{OUTPUT} is the period of the output signal produced by multiphase VCO 18, and x is the number of phases of the output signal (e.g., here x has a value of eight). Equation (1) above may be obtained from equation (3) by substituting $1/f_{FEEDBACK}$ for $T_{FEEDBACK}$, substituting $1/f_{OUTPUT}$ for T_{OUTPUT}, and solving for $f_{FEEDBACK}$. By reversing the direction of phase-switching, finite state machine 50 may operate to increase the delay through multiphase counter 20. That is, the following relationship between f_{OUT} and $f_{FEEDBACK}$ may be established:

$$f_{FEEDBACK} = f_{OUT} / (N + P/x) \quad (4)$$

Thus, during each feedback signal period, multiphase counter 20 produces a feedback signal pulse shifted in time by a programmable fraction (P/x) of the output signal period relative to the Nth output signal pulse of that period.

Referring to FIG. 5, in one embodiment, charge pump 14 includes a pull up current source 60, a pull down current source 62, and an equalization circuit 64 that is configured to substantially offset mismatches between pull up current source 60 and pull down current source 62. In particular, equalization circuit 64 includes a pull up offset cancellation current source 66 and a pull down offset cancellation current source 68 respectively coupled in parallel with pull up current source 60 and pull down current source 62. Frequency synthesizer 10 may be calibrated by adjusting an offset control signal (V_{OFFSET}) – which is applied to the inputs of offset cancellation current sources 66, 68 – until the pull up current ($I_{PULL\ UP}$) substantially equals the pull down current ($I_{PULL\ DOWN}$) (e.g., when the difference between $I_{PULL\ UP}$ and $I_{PULL\ DOWN}$ is within a selected tolerance value). This feature reduces jitter in the output signal generated by multiphase VCO 18 by substantially canceling layout and process related mismatches between up and down charges on loop filter 16.

Referring to FIG. 6, in one embodiment, frequency synthesizer 10 may include output stages 70, 72, which are configured to produce a sampling clock signal 74 (f_1) and an over-sampling clock signal 76 (f_2), respectively. Output stage 70 includes a frequency divider configured to divide the output signal frequency (f_{OUT}) by (M+1) to produce a frequency f_1:

$$f_1 = f_{OUT} / (M+1) = f_{REF} \cdot (N - P/x)/(M+1) \quad (5)$$

In this embodiment, a wide range of frequencies (f_1) may be synthesized while, at the same time, significantly reducing the dynamic range of the output signal. For example, in one

embodiment, a frequency range of 100 MHz to 800 MHz may be synthesized from an output signals with a dynamic range of one octave. In particular, by adjusting the value of M between, 0, 1 and 3, the following frequency ranges may be synthesized:

M	FREQUENCY RANGE
0	400-800 MHz
1	200-400 MHz
3	100-200 MHz

Output stage 72 includes a phase shifter 78 that is configured to increase the output frequency by a factor x/(x-1), and a frequency divider 80 that is configured to divide the output signal frequency (f_{OUT}) by (M+1) to produce a frequency f_2:

$$f_2 = x/(x-1) \cdot [f_{OUT} / (M+1)] = x/(x-1) \cdot [f_{REF} \cdot (N - P/x)/(M+1)] \quad (6)$$

Clock signals 74, 76 may be used in applications where a fixed relationship between f_1 and f_2 is desired. For example, clock signals 74, 76 may be used to respectively clock a read channel and a write channel for magnetic hard drive applications.

Other embodiments are within the scope of the claims.

WHAT IS CLAIMED IS:

1. A frequency synthesizer (10) for producing a series of output signal pulses spaced-apart by a characteristic period, comprising a phase-locked loop (11) having a multiphase counter (20) configured to produce a feedback signal pulse shifted in time by a programmable fraction of the output signal period relative to a period corresponding to a programmable number of output signal pulses.

2. The frequency synthesizer of claim 1, wherein the phase-locked loop (11) comprises an output signal generator (18) configured to produce multiple phases of the output signal.

3. The frequency synthesizer of claim 2, wherein the output signal generator (18) comprises a ring oscillator (18).

4. The frequency synthesizer of claim 2, wherein the multiphase counter (20) comprises a phase selector (40) coupled to the output signal generator (18) and configured to output a selected phase of the output signal based upon a programmable input value.

5. The frequency synthesizer of claim 4, wherein the phase selector (40) comprises a multiplexer (48) coupled to receive the multiple phases produced by the output signal generator (18).

6. The frequency synthesizer of claim 4, wherein the phase selector (40) comprises a finite state machine (50) having one state for each of the multiple phases of the output signal.

7. The frequency synthesizer of claim 6, wherein the finite state machine (50) is configured to switch states in response to a pulse of the selected phase of the output signal received from the multiplexer (48).

8. The frequency synthesizer of claim 4, wherein the multiphase counter (20) comprises a delay module (42) coupled to the phase selector (40) and configured to produce a feedback signal pulse after a programmable number of output signal pulses have been received from the phase selector (40).

9. The frequency synthesizer of claim 8, wherein the delay module (42) comprises a frequency divider.

10. The frequency synthesizer of claim 8, wherein the multiphase counter (20) comprises a controller (44) coupled to the phase selector (40) and configured to selectively enable and disable the phase selector (40).

11. The frequency synthesizer of claim 10, wherein the controller (44) is configured to enable the phase selector (40) upon receipt of a feedback signal pulse from the delay module (42).

12. The frequency synthesizer of claim 10, wherein the controller (44) is configured to disable the phase selector (40) after a programmable number of output signal pulses have been received from the phase selector (40).

13. The frequency synthesizer of claim 2, further comprising a phase shifter (50) coupled to the output signal generator (18) and configured to provide an over sampling clock signal with a frequency greater than the frequency of the output signal.

14. The frequency synthesizer of claim 1, wherein the phase-locked loop (11) comprises a charge pump (14) having a pull up current source (60), a pull down current source (62), and an equalization circuit (64) programmable to substantially offset mismatch between the pull up current source (60) and the pull down current source (62).

15. The frequency synthesizer of claim 14, wherein the equalization circuit (64) comprises a pull up offset cancellation current source (66) and a pull down offset cancellation current source (68) respectively coupled in parallel with the pull up and pull down current sources (60, 62).

16. A frequency synthesizer, comprising a phase-locked loop (11) having a charge pump (14) having a pull up current source (60), a pull down current source (62), and an equalization circuit (64) programmable to substantially offset mismatch between the pull up current source (60) and the pull down current source (62).

17. The frequency synthesizer of claim 16, wherein the equalization circuit (64) comprises a pull up offset cancellation current source (66) and a pull down offset cancellation current source (68) respectively coupled in parallel with the pull up current source (60) and the pull down current source (62).

18. A frequency synthesis method for producing a series of output signal pulses spaced-apart by a characteristic period, comprising:

generating the output signal pulses based upon a comparison of a reference signal and a feedback signal comprising a series of pulses; and

producing a feedback signal pulse shifted in time by a programmable fraction of the output signal period relative to a period corresponding to a programmable number of output signal pulses.

19. The method of claim 18, further comprising producing multiple phases of the output signal.

20. The method of claim 19, further comprising outputting a selected phase of the output signal based upon a programmable input value.

21. The method of claim 20, further comprising producing a feedback signal pulse after a programmable number of output signal pulses have been received.

22. The method of claim 19, further comprising providing an over sampling clock signal with a frequency greater than the frequency of the output signal.

23. The method of claim 18, further comprising substantially offsetting mismatch between a pull up current source (60) and a pull down current source (62) in a charge pump (14).

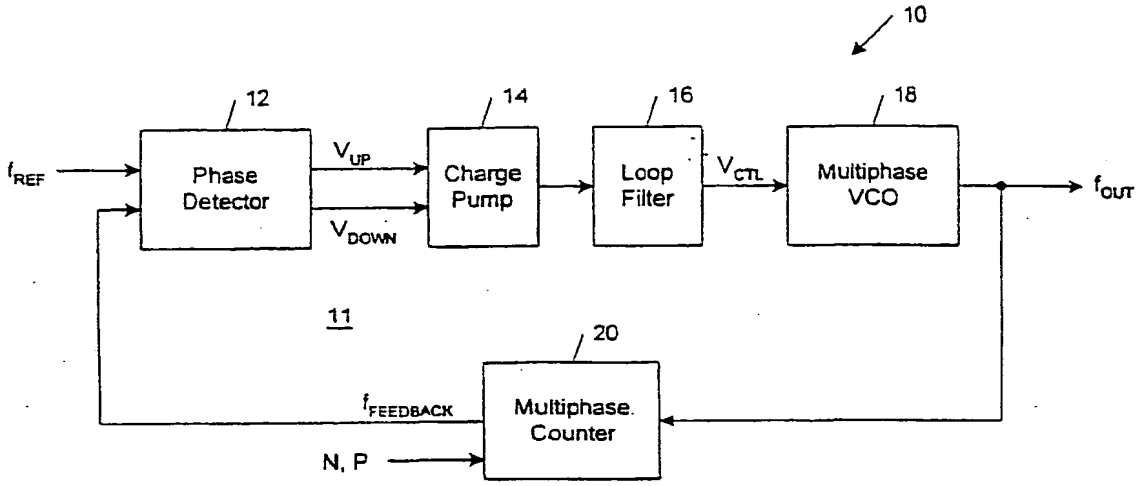


FIG. 1

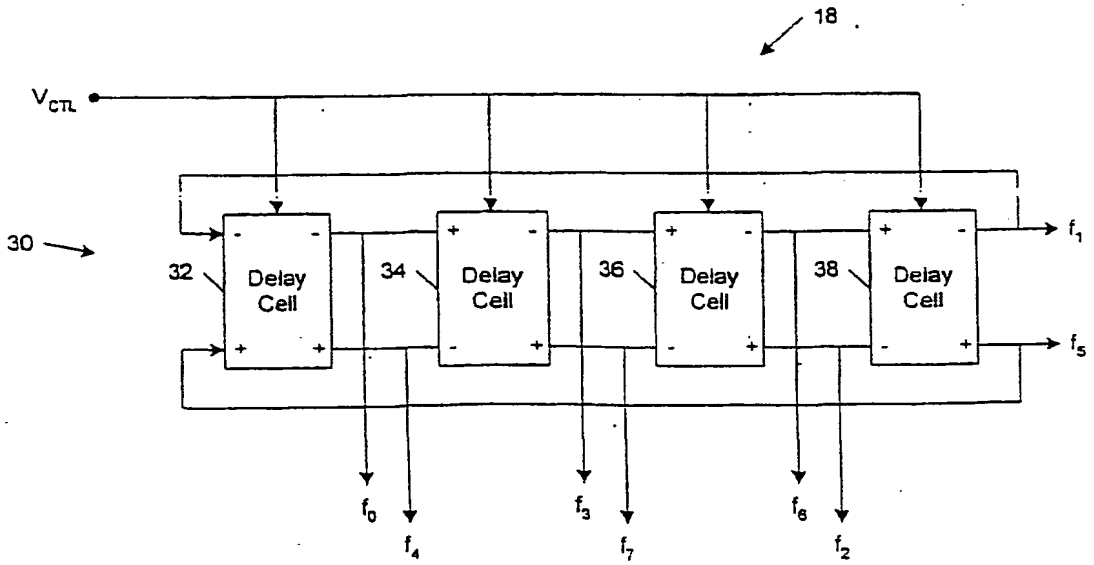


FIG. 2

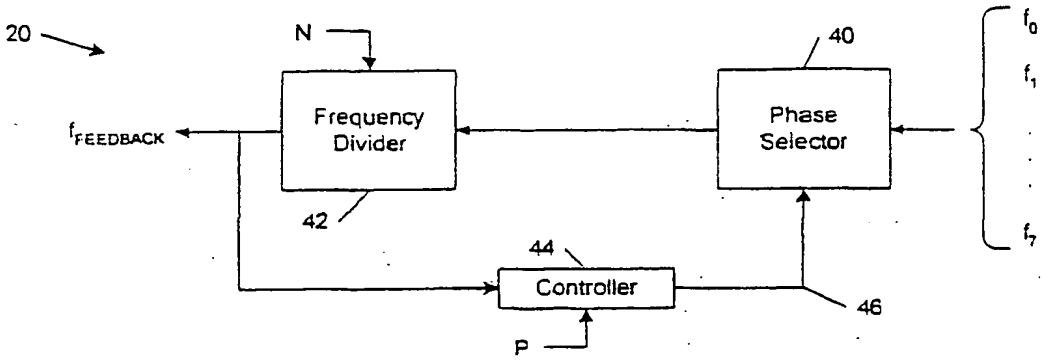


FIG. 3

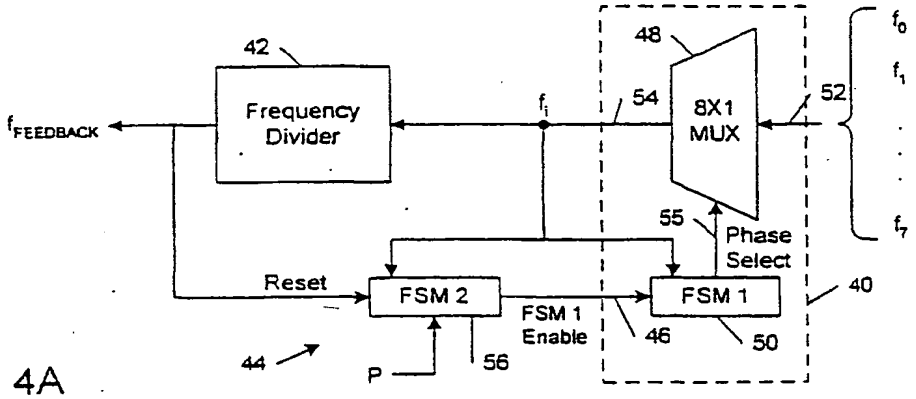


FIG. 4A

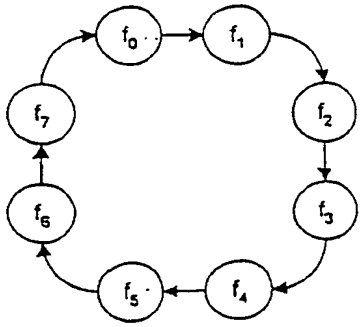


FIG. 4B

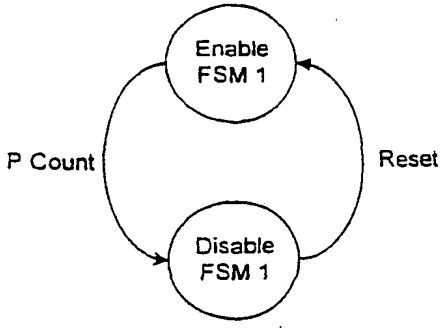


FIG. 4C

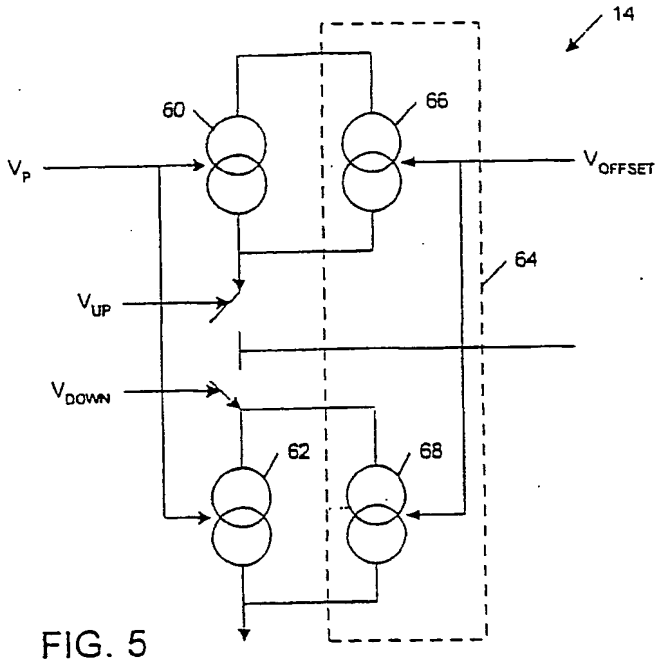

14
60
66
V_P
V_{OFFSET}
64
V_{UP}
V_{DOWN}
62
68

FIG. 5

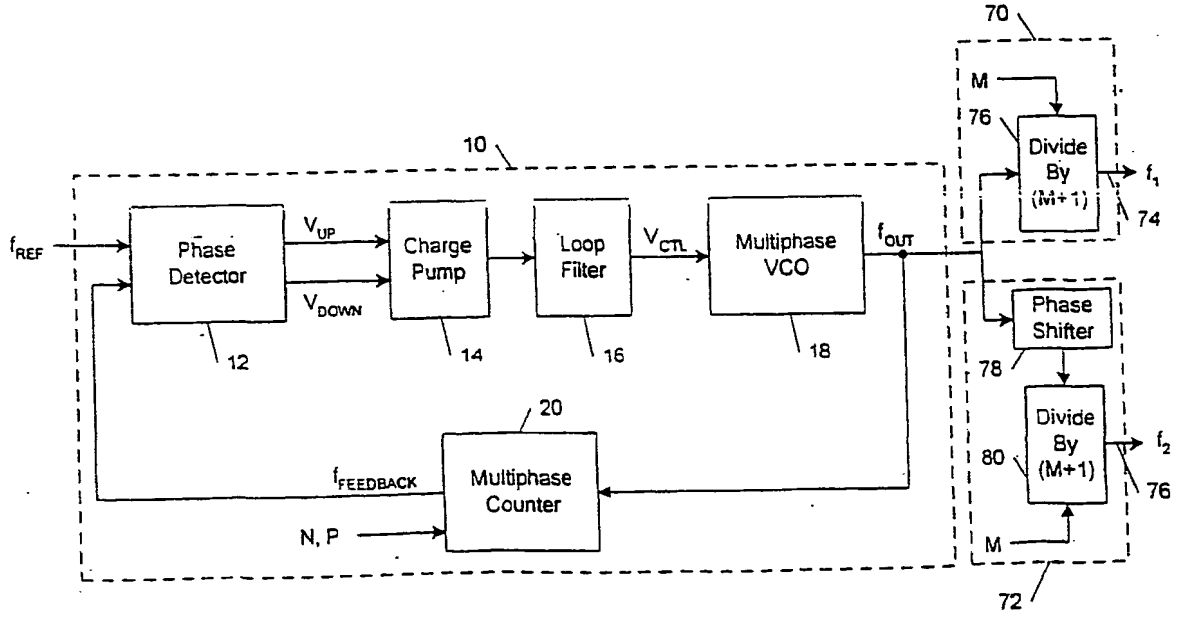

70
M
76
Divide By (M+1)
f_1
74
10
f_{REF}
Phase Detector
V_{UP}
V_{DOWN}
Charge Pump
Loop Filter
V_{CTL}
Multiphase VCO
f_{OUT}
12
14
16
18
Phase Shifter
78
Divide By (M+1)
f_2
80
76
M
20
$f_{FEEDBACK}$
Multiphase Counter
N, P
72

FIG. 6

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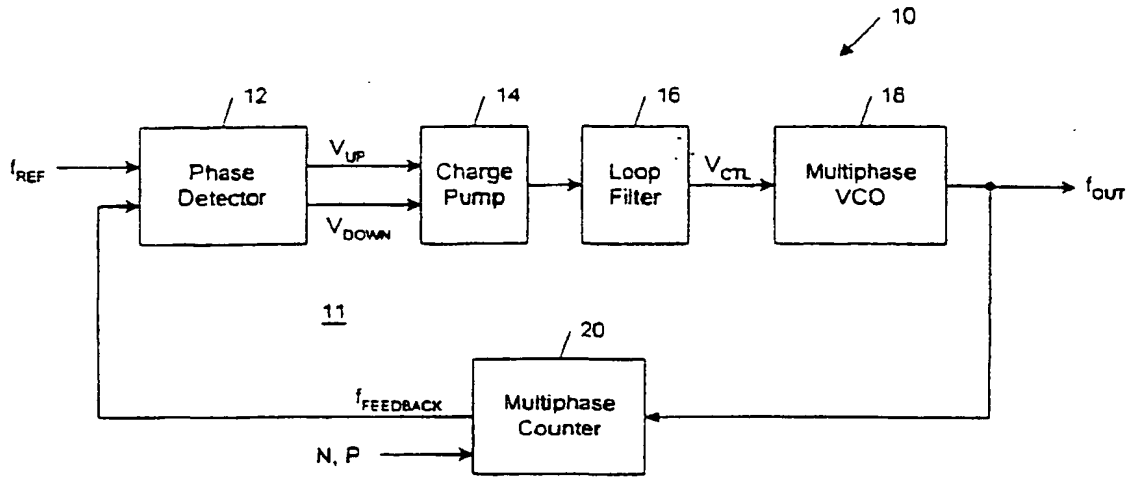
(54) Title: HIGH RESOLUTION, LOW JITTER FREQUENCY SYNTHESIZER



(57) Abstract: Systems and methods for synthesizing frequencies with high solution and low jitter are described. In one aspect, a frequency synthesizer (10)for producing a series of output signal pulses spaced-apart by a characteristic period is described. The frequency synthesizer includes a phase-locked looped (11)having a multiphase counter (20) configured to produce a feedback signal pulse shifted in time by a programmable fraction of the output signal period relative to a period corresponding to a programmable number of output signal pulses. In another aspect, a hase shifter is configured to provide an over sampling clock signal with a frequency greater than the frequency of the output signal. In another aspect, the frequency synthesizer includes a phase-locked loop with a charge pump (14)having a pull up current source, a pull down current source, and an equalization circuit programmable to substantially offset mismatch between the pull up current source and the pull down current source.

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According to International Patent Classification (IPC) or to both national classification and IPC

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Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 889 436 A (WONG KERN WAI ET AL) 30 March 1999 (1999-03-30) column 6, line 26 -column 8, line 64; figures 8-13	1-10,13, 18-22
Y		14,15,23
X	US 6 114 914 A (MAR MONTE F) 5 September 2000 (2000-09-05) column 3, line 14 -column 5, line 26; figures 4,5	1-4,6,8, 18-21
Y		14,15,23
X	US 5 059 924 A (JENNINGSCHECK WILLIAM S) 22 October 1991 (1991-10-22) column 4, line 6 -column 7, line 66; claim 14; figures 1,2,6	1-10,13, 18-22
Y		14,15,23

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
10 July 2002	17/07/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Balbinot, H

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/24648

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 111 468 A (TANISHIMA HIDEAKI) 29 August 2000 (2000-08-29) column 13, line 66 -column 20, line 7 column 23, line 35 -column 24, line 37 column 25, line 63 -column 27, line 15 figures 17,20,27,29,30	16,17
Y	-----	14,15,23

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 01/24648

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-15,18-23

   Frequency synthesizer comprising a phase locked loop having a multiphase counter producing a feedback signal pulse shifted in time by a programmable fraction of the output signal period relative to a period corresponding to a programmable number of output signal pulses.

2. Claims: 16, 17

   Frequency synthesizer comprising a phase-locked loop having a charge pump provided with an equalization circuit programmable to substantially offset mismatch the up and down current sources of the charge pump.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/24648

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5889436	A	30-03-1999	NONE		
US 6114914	A	05-09-2000	NONE		
US 5059924	A	22-10-1991	CA	2002382 A1	07-05-1990
			WO	9006017 A1	31-05-1990
US 6111468	A	29-08-2000	JP	11225069 A	17-08-1999
			TW	415147 B	11-12-2000

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